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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/578,003	05/03/2006	Hideo Nakagawa	071971-0548	5215
53080 7590 01/22/2009 MCDERMOTT WILL & EMERY LLP 600 13TH STREET, NW WASHINGTON, DC 20005-3096				
EXAMINER				
WILLIAMS, ALEXANDER O				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/578,003

**Applicant(s)**

NAKAGAWA ET AL.

**Examiner**

Alexander O. Williams

**Art Unit**

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 25 October 2008.  
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1, 2, 4-51, 54 and 55 is/are pending in the application.  
4a) Of the above claim(s) 2, 4, 5 and 8-51 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1, 6, 7, 54 and 55 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

Serial Number: 10/578003 Attorney's Docket #: 071971-0548  
Filing Date: 5/3/2006; claimed foreign priority to 6/3/2004

Applicant: Nakagawa et al.

Examiner: Alexander Williams

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/15/08 has been entered.

Applicant's Amendment filed 10/15/08 to the election of Species II, identifying figures 2a and 2b (claims 1, 3, 6 and 7), filed 10/23/2007, has been acknowledged.

Claims 3, 52 and 53 have been cancelled.

This application contains claims 2, 4, 5 and 8-51 drawn to an invention non-elected without traverse.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:  
A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 6, 7 and 54 are rejected under 35 U.S.C. § 102(e) as being anticipated by Saito et al. (U.S. Patent Application Publication # 2008/0230916 A1).

1. Saito et al. (figures 1-63) specifically figure 1 show a semiconductor device comprising: an insulation film **4b2** formed on a substrate **1**; a buried metal interconnect **10C2** formed in the insulation film; and a barrier metal film **9L** formed between the insulation film and the metal interconnect, wherein the barrier metal film is a metal compound film, and wherein the metal compound film contains at least one of elements forming the insulation film and is made of at least one selected from consisting of Zr, Hf, **W**, V, Mo, Os, Rh, Ir, Pd and Pt or **any alloy thereof**.

6. The semiconductor device of claim 1, Saito et al. show wherein a metal forming the metal compound film is a refractory metal.
7. The semiconductor device of claim 1, Saito et al. show wherein the metal interconnect is formed of copper or an copper alloy.
54. The semiconductor device of claim 1, Saito et al. show wherein the insulation film is SiO<sub>2</sub>.

Claims 1, 6, 7, 54 and 55 are rejected under 35 U.S.C. § 102(e) as being anticipated by Saito et al. (U.S. Patent Application Publication # 2003/0109129 A1).

1. Saito et al. (figures 1-63) specifically figure 19 show a semiconductor device comprising: an insulation film **36** formed on a substrate **1**; a buried metal interconnect **M4** formed in the insulation film; and a barrier metal film **PM5a** formed between the insulation film and the metal interconnect, wherein the barrier metal film is a metal compound film, and wherein the metal compound film contains at least one of elements forming the insulation film and is made of at least one selected from consisting of Zr, Hf, **W**, V, Mo, Os, Rh, Ir, Pd and Pt or **any alloy thereof**.

6. The semiconductor device of claim 1, Saito et al. show wherein a metal forming the metal compound film is a refractory metal.
7. The semiconductor device of claim 1, Saito et al. show wherein the metal interconnect is formed of copper or an copper alloy.
54. The semiconductor device of claim 1, Saito et al. show wherein the insulation film is SiO<sub>2</sub> (paragraphs [0032] and [0038]).

55. The semiconductor device of claim 1, Saito et al. show wherein the insulation film is nitride (paragraphs [0032] and [0038]).

[0024] (2-4) The manufacturing method of a semiconductor device as described above in (2-1), wherein the barrier metal layer is formed from a single layer film of any one of Ta, TaN, TaSiN, W, WN, WSiN, Ti, TiN and TiSiN; or a laminate film obtained by stacking a plurality of any two or greater of Ta, TaN, TaSiN, W, WN, WSiN, Ti, TiN and TiSiN.

Summary of Invention Paragraph - BSTX (27):

[0025] (2-5) The manufacturing method of a semiconductor device as described above in (2-1), wherein the capping barrier metal film is formed from a metal layer composed mainly of W, WN, WSiN and W, a metal layer composed mainly of CoWP, CoWB or Co, a single layer film of any one of TiN, TiSiN, Ta, TaN and TaSiN, or a laminate film obtained by stacking any two of the metal layers and single layer films.

Summary of Invention Paragraph - BSTX (34):

[0032] (5-4) The manufacturing method of a semiconductor device as described above in (5-3), wherein the low dielectric constant film is a film formed by CVD by using Si and C, Si and N, Si, C and N, Si, O and N, Si, O and C, Si, O, C and N, or TMS and N.sub.2O.

Summary of Invention Paragraph - BSTX (40):

[0038] (5-10) The manufacturing method of a semiconductor device as described above in (5-9), wherein: the low dielectric constant film has Si and C, Si, C and O, Si, O and F, C and H, or Si, O, C and H; or in addition, is porous.

Claims 1, 6, 7, 54 and 55 are rejected under 35 U.S.C. § 102(b) as being anticipated by Ohtsuka et al. (U.S. Patent Application Publication # 2002/0019131 A1).

1. Ohtsuka et al. (figures 1A-4B) specifically figure 3C show a semiconductor device comprising: an insulation film **21** formed on a substrate **10**; a buried metal interconnect **24** formed in the insulation film; and a barrier metal film **22** formed between the insulation film and the metal interconnect, wherein the barrier

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metal film is a metal compound film , and wherein the metal compound film contains at least one of elements forming the insulation film and is made of at least one selected from consisting of **Zr**, **hf**, **W**, **V**, **Mo**, **Os**, **Rh**, **Ir**, **Pd** and **Pt** or **any alloy thereof**.

6. The semiconductor device of claim 1, Ohtsuka et al. show wherein a metal forming the metal compound film is a refractory metal.

7. The semiconductor device of claim 1, Ohtsuka et al. show wherein the metal interconnect is formed of copper or an copper alloy.

54. The semiconductor device of claim 1, Ohtsuka et al. show wherein the insulation film is SiO<sub>2</sub>.

55. The semiconductor device of claim 1, Ohtsuka et al. show wherein the insulation film is nitride.

[0052] Barrier layer is preferably formed of refractory metal such as Ti, Ta, W, Mo, Zr or their nitride. If the barrier layer is formed by CVD, a TiN layer, a WN layer, or a ZrN layer may be used as the barrier layer. A TaN layer is also expected to be usable.

## Response

Applicant's arguments filed 10/15/08 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander O Williams/  
Primary Examiner, Art Unit 2826

AOW  
1/22/2009